Amendments to the Specification:

Please replace paragraph [0051] wit the following paragraph:

[0051] During the read and write operations, the desired memory cell **30** must be accessed. The row address decoder **22** accepts control and address signals directly from a processor (not shown) or memory controller (not shown) over a row address input bus. 'Directly' refers to a signal that is exchanged between the processor and a specific memory array without ~~needed~~ needing a multiplexer. The row address decoder **22** decodes the signals and activates its word line **26** (i.e., row address output bus), thereby selecting one or more desired rows of memory cells **30**. Each memory cell **30** within an activated row outputs its data to its corresponding bit line.